Docket No. SC10927TS

REMARKS

Claims 1-6, 8-9, 11-17, and 19-22 will be pending in the current Application upon entering this Amendment. Claims 1, 8, and 9 have been amended and claim 10 has been cancelled herein. (Note that claims 7 and 18 were previously cancelled.) Applicant submits that the amendments do not add new matter to the current Application. Applicant also wishes to thank the Examiner for pointing out allowable subject matter (including claims 6, 17, 14-16, and 22).

All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicant also submits that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Rejection of claims 1-6, 8-9, 12-16, and 18-22 under 35 U.S.C. 103(a)

Applicant respectfully submits that claims 1-6, 8-9, 12-16, and 18-22 are patentable over US Patent No. 5, 701, 495 (hereinafter referred to as Arndt) in view of US Patent No. 6,185,629 (hereinafter referred to as Simpson).

Claim 1

Applicant submits that claim 1, as amended, is allowable over Arndt in view of Simpson. Applicant has amended claim 1 to further clarify the element of "assigning an interrupt prioritization level to storage locations of the first storage device and the second storage device," by amending this element to read "assigning an interrupt prioritization level to each of a plurality of storage locations of the first device and to each of a plurality of storage locations of the second storage device." That is, claim 1 requires that interrupt prioritization levels be assigned to each of a plurality of storage locations in the first storage device ***and*** to each of a plurality of storage locations in the second storage device. Applicant submits that neither Arndt, Simpson, nor their combination teach or suggest assigning an interrupt prioritization level as claimed in claim 1. The Examiner, in the Response to Arguments Section in the current Office Action states that

(with respect to the previous element of claim 1 stating "assigning an interrupt prioritization level to storage locations of the first storage device and the second storage device") Arndt teaches this because "since the step of selecting the highest priority by routing layer 55 between the storage interrupts queues 56 and 57, it is inherently implying the layer 55 is assigning an interrupt prioritization level between the two." However, Applicant has amended claim 1 to further clarify that claim 1 is not simply claiming assigning a prioritization level by determining which queue to select (as the Examiner asserts that routing layer 55 does in selecting one of queues 56 and 57), but claim 1 is claiming assigning a prioritization level to each of a plurality of storage locations *in each storage device*. That is, Arndt does not teach or suggest assigning a prioritization level to each of a plurality of storage locations of queue 56 and to each of a plurality of storage locations of queue 57, such that a plurality of specific storage locations in *each* of the queues has a specific prioritization level, regardless of what is stored in those storage locations. Furthermore, Applicant submits that bit fields 24-31 of the XIVR register also do not teach or suggest this element of claim 1. As stated in Applicant's previous response, bits 24-31 allow an interrupt priority to be assigned to a particular interrupt; however, these bits do not assign an interrupt prioritization to storage locations of queues 56 and 57. Bits 24-31 within the interrupt vector register in the IOCs allow for specifying different priorities for specific interrupts, as needed, but does not teach or suggest assigning an interrupt prioritization level to a plurality of storage locations of queue 56 and to a plurality of storage locations of queue 57, as required by claim 1. Therefore, for at least those reasons, Applicant submits that claim 1 is allowable over Arndt in view of Simpson. Claims 2-6 depend directly or indirectly from allowable claim 1 and are therefore allowable for at least those reasons mentioned above with respect to claim 1.

Claim 8

Applicant submits that claim 8 is allowable over Arndt in view of Simpson because neither Arndt, Simpson, nor their combination teach or suggest each and every limitation of claim 8. For example, claim 8 has also been amended to further clarify the element of "assigning an interrupt prioritization level to storage locations of the first storage device and the second storage device" by amending this element to read "assigning an interrupt prioritization level to

each of a plurality of storage locations of the first device and to each of a plurality of storage locations of the second storage device." Neither Arndt, Simpson, nor their combination teach or suggest this limitation. As discussed above in reference to claim 1, routing layer 55, by selecting between queues 56 and 57, does not teach or suggest assigning an interrupt prioritization level to a plurality of storage locations of queue 56 *and* to a plurality of storage locations of queue 57. Also, as discussed above with reference to claim 1, bits 24-31 within the interrupt vector register in the IOCs allow for specifying different priorities for specific interrupts, as needed, but does not teach or suggest assigning an interrupt prioritization level to a plurality of storage locations of each of a first and second storage device, as claimed in claim 8. Therefore, for at least these reasons, Applicant submits that claim 8 is patentable over Arndt in view of Simpson.. Claims 19-21 depend from claim 8, and are therefore allowable for at least those reasons described above with reference to claim 8.

Furthermore, as stated in Applicant's previous response, claim 19 further requires assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from some interrupt sources generating hardware interrupts and having a corresponding interrupt prioritization level. Arndt, at col. 4, lines 25-32, discusses software queues which store events comprising hardware generated interrupts and software generated interrupts, but there is no teaching or suggestion of assigning a portion of the plurality of software-generated interrupt signals to represent interrupts from sources generating hardware interrupts, as claimed in claim 19. Therefore, claim 19 is also allowable over Arndt in view of Simpson for these additional reasons.

Claim 9

Applicant submits that claim 9 is allowable over Arndt in view of Simpson because neither Arndt, Simpson, nor their combination teach or suggest each and every limitation of claim 9. However, in order to further prosecution and not for prior art reasons, Applicants have amended claim 9 to include the limitations of dependent claim 10. Therefore, claim 9 now further claims each of the hardware interrupt storage device and the software interrupt storage device having an assigned interrupt prioritization level to specific storage locations, the interrupt prioritization level of the hardware interrupt sources being permanently assigned, but assignment of the interrupt prioritization level of interrupt sources associated with the software-generated interrupt signals being variable by software control . Neither Arndt, Simpson, nor their

combination teach or suggest this limitation . The Examiner has agreed that the cited references do not teach or suggest this element since the Examiner has indicated in the current Office Action that claim 17 would be allowable if rewritten in independent form, and dependent claim 17 includes the same limitations as dependent claim 10. Furthermore, as stated in Applicant's previous response, the cited references do not teach or suggest the limitations of dependent claim 10. For example, col. 4, lines 53-61 of Arndt simply discusses the existence of a server number associated with each queue 42, 43, but does not teach or suggest this element of claim 10 (which is now included in claim 9). Therefore, for at least these reasons, Applicant submits that claim 9 is allowable over the cited references. Claims 11-13 depend directly or indirectly from allowable claim 9 and are therefore allowable for at least those reasons mentioned above with respect to claim 9.

Conclusion

Although Applicant may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicant is not discussing all these statements in the current Office Action, yet reserves the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

Please charge any fees due to **Deposit Account Number 502117, Motorola, Inc.**.

Respectfully submitted,

By: _____

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